

PALCE26V12H-20/25

28-Pin EE CMOS Versatile PAL[®] Device



PALCE26V12H-20/25

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- 28-pin versatile PAL[®] programmable logic device architecture
- Electrically erasable CMOS technology provides half power (only 105 mA) at high speed (20 ns propagation delay)
- Replaces discrete CMOS/TTL logic, reducing design time and cost and increasing reliability
- 14 dedicated inputs and 12 input/output macrocells for architectural flexibility
- Macrocells can be registered or combinatorial, and active HIGH or active LOW to match application needs
- Varied product term distribution allows up to 16 product terms per output for complex functions
- Two clock inputs for independent registered functions
- Global asynchronous reset and synchronous preset for initialization
- Register preload for testability and built-in register reset on power-up
- Security bit prevents design duplication by competitors
- Space-efficient 28-pin SKINNYDIP[®] and PLCC packages
- Center VCC and GND pins to improve signal characteristics
- Supported by PALASM[®] 2 software and other design tools and standard logic programmers
- Fully tested for high programming and functional yields and high reliability

GENERAL DESCRIPTION

The PALCE26V12H is a 28-pin version of the popular PAL22V10 architecture. Built with low-power, high-speed, electrically-erasable CMOS technology, the PALCE26V12H offers many unique advantages.

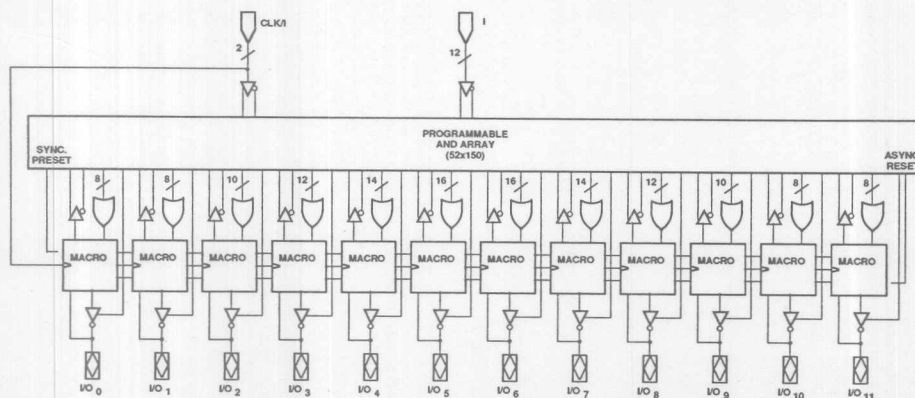
Device logic is automatically configured according to the user's design specification. Design is simplified by PALASM 2 design software from AMD, allowing automatic creation of a programming file based on Boolean or state equations. PALASM 2 software also verifies the design and can provide test vectors for the programmed device. Third-party design tools and logic programmers also support the PALCE26V12H (see Programmers/Development Systems).

The PALCE26V12H utilizes the familiar sum-of-products (AND/OR) architecture that allows users to implement complex logic functions easily and efficiently. Multiple

levels of combinatorial logic can always be reduced to sum-of-products form, taking advantage of the very wide input gates available in PAL devices. The functions are programmed into the device through electrically-erasable floating-gate cells in the AND logic array and the macrocells. In the unprogrammed state, all AND product terms float HIGH. If both true and complement of any input are connected, the term will be permanently LOW.

The product terms are connected to the fixed OR array with a varied distribution from 8 to 16 across the outputs (see Block Diagram). The OR sum of the products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial, active HIGH or active LOW, with registered I/O possible. The flip-flop can be clocked by one of two clock inputs. The output configuration is determined by four bits controlling three multiplexers in each macrocell.

BLOCK DIAGRAM



11757-001A

BD008380

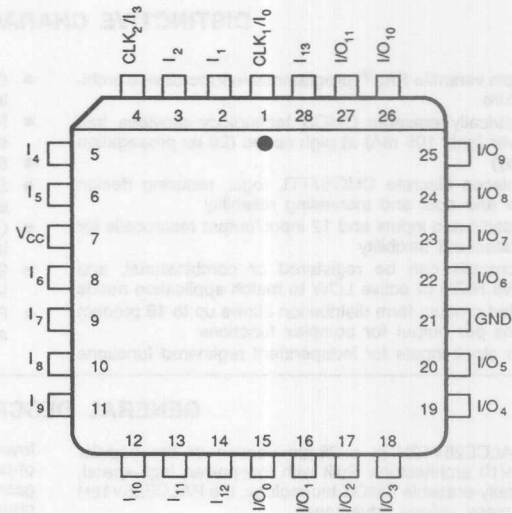
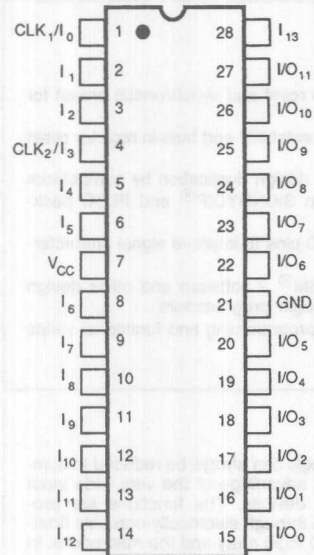
PAL, PALASM, and SKINNYDIP are registered trademarks of Advanced Micro Devices.
This part is covered by various U.S. and foreign patents owned by Advanced Micro Devices.

Publication # 11757 Rev. A
Issue Date: January 1989

CONNECTION DIAGRAMS Top View

SKINNYDIP

PLCC



11757-005A
CD011890

11757-007A
CD011900

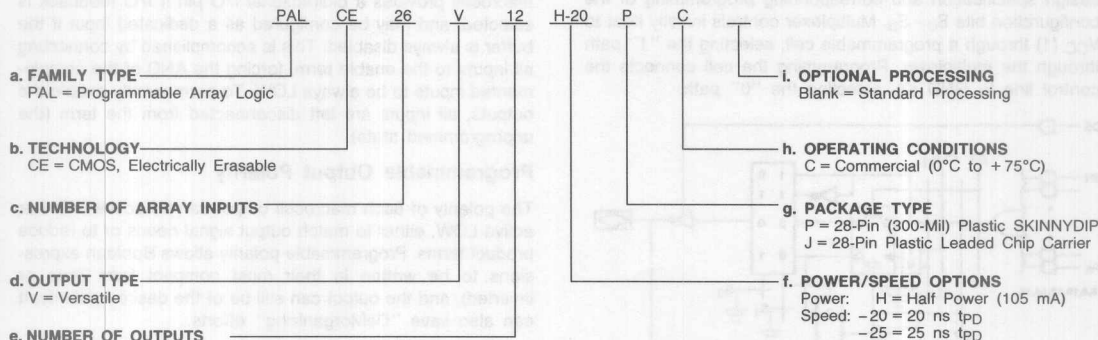
Pin Designations: I = Input
I/O = Input/Output
CLK = Clock
V_{CC} = Supply Voltage
GND = Ground

ORDERING INFORMATION

Programmable Array Logic (PAL) Products

AMD PAL products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. Family Type
- b. Technology
- c. Number of Array Inputs
- d. Output Type
- e. Number of Outputs
- f. Power/Speed Options
- g. Package Type
- h. Operating Conditions
- i. Optional Processing



Valid Combinations	
PALCE26V12H-20	PC, JC
PALCE26V12H-25	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

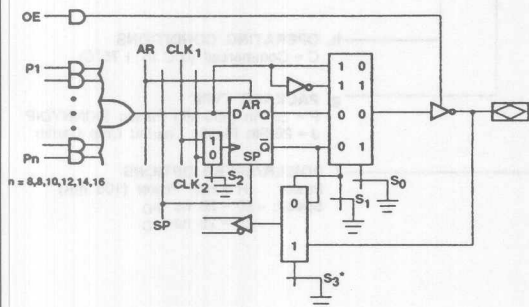
Note: Marked with AMD logo

FUNCTIONAL DESCRIPTION

The PALCE26V12H has fourteen dedicated input lines, two of which can be used as clock inputs. Unused inputs should be tied directly to ground or V_{CC} . Buffers for device inputs and feedbacks have both true and complementary outputs to provide user-selectable signal polarity. The inputs drive a programmable AND logic array, which feeds a fixed OR logic array.

The OR gates feed the twelve I/O macrocells (see figure 1). The macrocell allows one of eight potential output configurations; registered or combinatorial, active HIGH or active LOW, with register or I/O pin feedback (see figure 2). In addition, registered configurations can be clocked by either of the two clock inputs.

The configuration choice is made according to the user's design specification and corresponding programming of the configuration bits $S_0 - S_3$. Multiplexer controls initially float to V_{CC} (1) through a programmable cell, selecting the "1" path through the multiplexer. Programming the cell connects the control line to GND (0), selecting the "0" path.



11757-000A
LD001671

When $S_3 = 1$ (unprogrammed) the feedback is selected by S_1 .
When $S_3 = 0$ (programmed), the feedback is the opposite of that selected by S_1 .

Figure 1. PALCE26V12H Macrocell

Registered or Combinatorial

Each macrocell of the PALCE26V12H includes a D-type flip-flop for data storage and synchronization. The flip-flop is loaded on the LOW-to-HIGH edge of the selected clock input. Any macrocell can be configured as combinatorial by selecting a multiplexer path that bypasses the flip-flop. Bypass is controlled by bit S_1 .

Programmable Clock

The clock input for any flip-flop can be selected to be from either pin 1 or pin 4. A 2:1 multiplexer controlled by bit S_2 determines the clock input.

Programmable Feedback

A 2:1 multiplexer allows the user to determine whether the macrocell feedback comes from the flip-flop or from the I/O pin, independent of whether the output is registered or combinatorial. Thus, registered outputs may have internal register feedback for higher speed (t_{CF} specification applies), or I/O feedback for use of the pin as a direct input (t_{CO}

specification applies). Combinatorial outputs may have I/O feedback, either for use of the signal in other equations or for use as another direct input, or register feedback.

The feedback multiplexer is controlled by the same bit (S_1) that controls whether the output is registered or combinatorial, as on the 22V10, with an additional control bit (S_3) that allows the alternative feedback path to be selected. When $S_3 = 1$, S_1 selects register feedback for registered outputs ($S_1 = 0$) and I/O feedback for combinatorial outputs ($S_1 = 1$). When $S_3 = 0$, the opposite is selected: I/O feedback for registered outputs and register feedback for combinatorial outputs.

Programmable Enable and I/O

Each macrocell has a three-state output buffer controlled by an individual product term. Enable and disable can be a function of any combination of device inputs or feedback. The macrocell provides a bidirectional I/O pin if I/O feedback is selected, and may be configured as a dedicated input if the buffer is always disabled. This is accomplished by connecting all inputs to the enable term, forcing the AND of the complemented inputs to be always LOW. To permanently enable the outputs, all inputs are left disconnected from the term (the unprogrammed state).

Programmable Output Polarity

The polarity of each macrocell output can be active HIGH or active LOW, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts.

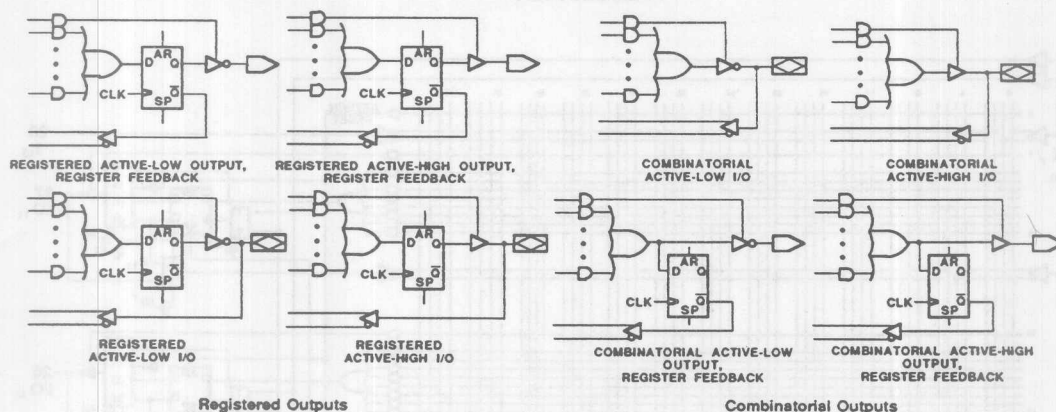
Selection is controlled by programmable bit S_0 in the output macrocell, and affects both registered and combinatorial outputs. Selection is automatic, based on the design specification and pin definitions. If the pin definition and output equation have the same polarity, the output is programmed to be active HIGH.

Note that preset and reset control the flip-flop, not the output pin. The output level is determined by the output polarity selected.

S_3	S_1	S_0	Output Configuration
1	0	0	Registered Output and Feedback, Active LOW
1	0	1	Registered Output and Feedback, Active HIGH
1	1	0	Combinatorial I/O, Active LOW
1	1	1	Combinatorial I/O, Active HIGH
0	0	0	Registered I/O, Active LOW
0	0	1	Registered I/O, Active HIGH
0	1	0	Combinatorial Output, Registered Feedback, Active LOW
0	1	1	Combinatorial Output, Registered Feedback, Active HIGH

S_2	Clock Input
1	CLK ₁ /I ₀
0	CLK ₂ /I ₃

1 = Unprogrammed EE bit
0 = Programmed EE bit



LD001690

Figure 2. PALCE26V12H Macrocell Configuration Options

Power-Up Reset

All flip-flops power up to a logic LOW for predictable system initialization. Outputs of the PALCE26V12H will be HIGH or LOW depending on whether the output is active LOW or active HIGH, respectively. The V_{CC} rise must be monotonic, and the reset delay time is 1 μ s maximum.

Register Preload

The register on the PALCE26V12H can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, thereby making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Bit

After programming and verification, a PALCE26V12H design can be secured by programming the security bit. Once

programmed, this bit defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. Programming the security bit disables preload.

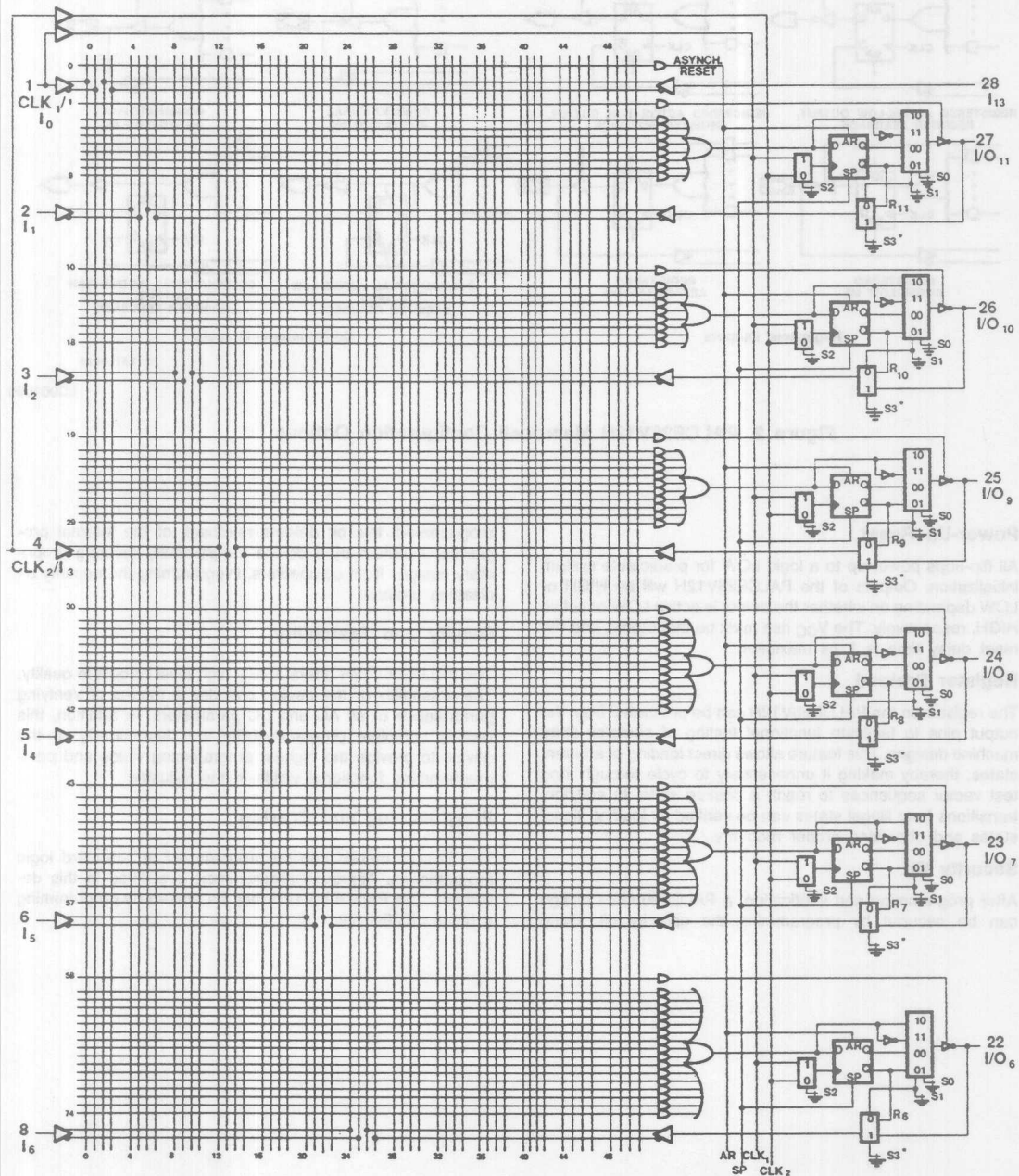
Quality and Testability

The PALCE26V12H offers a very high level of built-in quality. The erasability of the device provides a means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

Programming and Erasing

The PALCE26V12H can be programmed on standard logic programmers. Approved programmers are listed in this datasheet. The PALCE26V12H may be erased by programming a blank JEDEC file.

PALCE26V12H



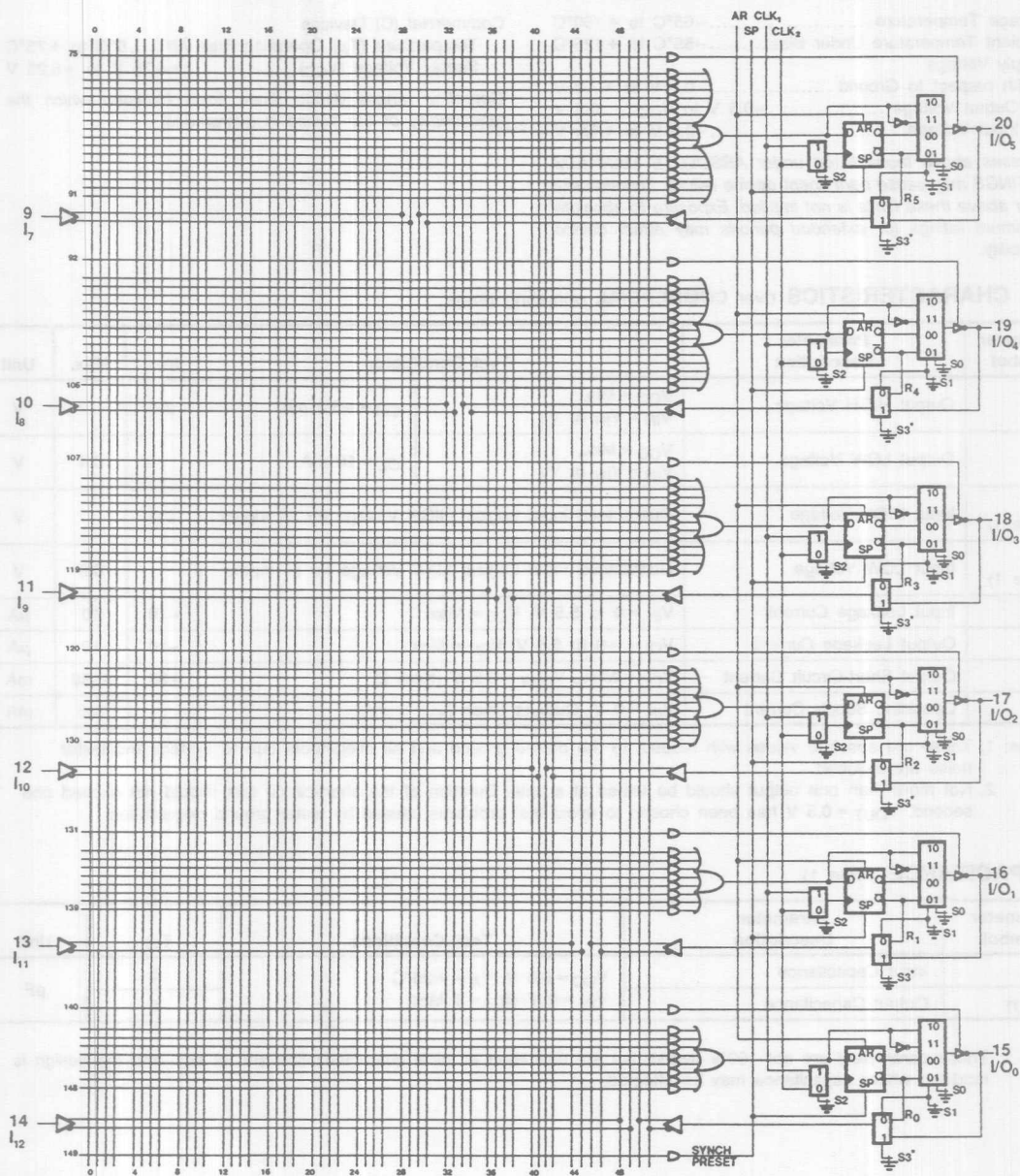
11757-006A

LD001740

*When $S_3 = 1$ (unprogrammed) the feedback is selected by S_1 .
 When $S_3 = 0$ (programmed), the feedback is the opposite of that selected by S_1 .

Figure 3. Logic Diagram

PALCE26V12H



11757-005A (Concluded)

LD001730

*When $S_3 = 1$ (unprogrammed) the feedback is selected by S_1 .

When $S_3 = 0$ (programmed), the feedback is the opposite of that selected by S_1 .

Figure 3. (Cont'd.)

ABSOLUTE MAXIMUM RATINGS

Storage Temperature -65°C to +150°C
 Ambient Temperature Under Bias -55°C to +125°C
 Supply Voltage
 with respect to Ground -0.5 V to +7.0 V
 DC Output Voltage -0.5 V to $V_{CC} + 0.5$ V
 DC Input Voltage -0.6 V to +7.0 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating Free Air 0°C to +75°C

Supply Voltage (V_{CC}) +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating range

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$, $V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -3.2$ mA	2.4		V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$, $V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 16$ mA		0.4	V
V_{IH} (Note 1)	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs	2.0		V
V_{IL} (Note 1)	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs		0.8	V
I_I	Input Leakage Current	$V_{IN} = 0$ to 5.5 V, $V_{CC} = \text{Max.}$	-10	10	μA
I_O	Output Leakage Current	$V_{OUT} = 0$ to 5.5 V, $V_{CC} = \text{Max.}$	-10	10	μA
I_{SC}	Output Short-Circuit Current	$V_{CC} = \text{Max.}$, $V_{OUT} = 0.5$ V (Note 2)	-30	-130	mA
I_{CC}	Operating Supply Current	$V_{IN} = 0$ V, Outputs Open ($I_O = 0$ mA)		105	mA

Notes: 1. These are absolute values with respect to the device ground and all overshoots due to system and tester noise are included.

2. Not more than one output should be tested at a time. Duration of the short-circuit test should not exceed one second. $V_{OUT} = 0.5$ V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Unit
C_{IN}	Input Capacitance	$V_{CC} = 5.0$ V, $T_A = +25^\circ\text{C}$ $V_{IN} = 0$ V @ $f = 1$ MHz	5	pF
C_{OUT}	Output Capacitance		8	

Note: 1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating range (Note 1)

Parameter Symbol	Parameter Description		-20		-25		Unit
			Min.	Max.	Min.	Max.	
t _{PD}	Input or Feedback to Combinatorial Output	Active LOW		20		25	ns
		Active HIGH					
t _S	Setup Time from Input, Feedback, or SP to Clock		13		15		ns
t _H	Hold Time		0		0		ns
t _{CO}	Clock to Output			12		15	ns
t _{CF}	Clock to Feedback			10		13	ns
t _{AR}	Asynchronous RESET to Registered Output			25		30	ns
t _{ARW}	Asynchronous RESET Width		20		25		ns
t _{ARR}	Asynchronous RESET Recovery Time		20		25		ns
t _{SPR}	Synchronous PRESET Recovery Time		13		15		ns
t _{WL}	Width of Clock	LOW	10		13		ns
t _{WH}		HIGH	10		13		ns
f _{MAX}	Maximum Frequency (Note 2)	External Feedback 1/(t _S + t _{CO})	40		33.3		MHz
		Internal Feedback 1/(t _S + t _{CF})	43		35		
t _{EA}	Input to Output Enable			20		25	ns
t _{ER}	Input to Output Disable			20		25	ns

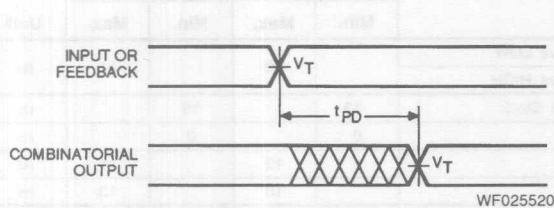
Notes: 1. Commercial Test Conditions: see Switching Test Load

2. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

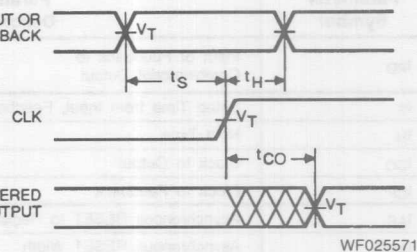
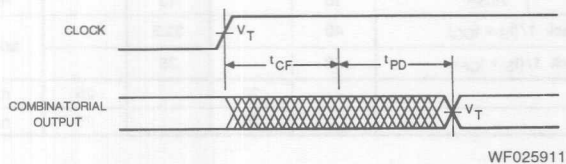
Endurance Characteristics

Symbol	Parameter	Value	Units	Test Conditions
t _{DR}	Min. Pattern Data Retention Time	10	Years	Max. Storage Temperature
N	Min. Reprogramming Cycles	100	Cycles	Operating Conditions

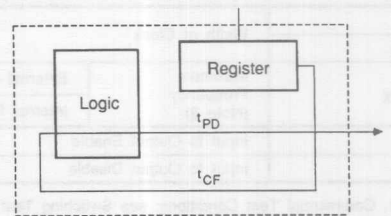
SWITCHING WAVEFORMS



Combinatorial Output

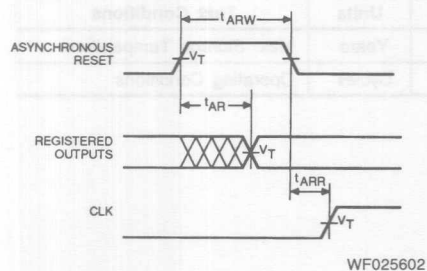


Registered Output

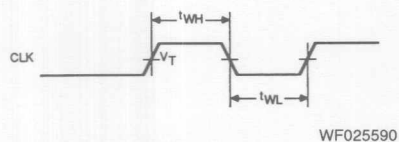


LD001720

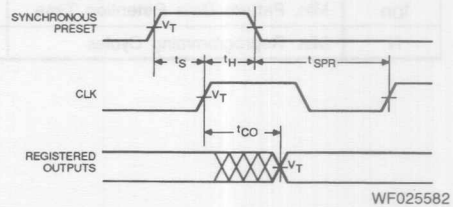
Clock to Feedback to Combinatorial Output (See Path at Right)



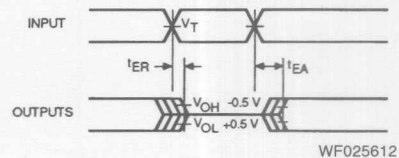
Asynchronous Reset



Clock Width



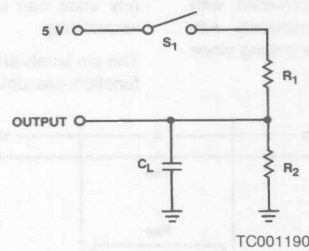
Synchronous Preset



Input to Output Disable/Enable

- Notes: 1. $V_T = 1.5 \text{ V}$
 2. Input pulse amplitude 0 V to 3.0 V
 3. Input rise and fall times 2–5 ns typical

SWITCHING TEST CIRCUIT



Specification	Switch S_1	C_L	R_1	R_2	Measured Output Value
t_{PD} , t_{CO} , t_{CF}	Closed	50 pF	300 Ω	390 Ω	1.5 V
t_{EA}	Z \rightarrow H: open Z \rightarrow L: closed	50 pF	300 Ω	390 Ω	1.5 V
t_{ER}	H \rightarrow Z: open L \rightarrow Z: closed	5 pF	300 Ω	390 Ω	H \rightarrow Z: $V_{OH} - 0.5$ V L \rightarrow Z: $V_{OL} + 0.5$ V

SWITCHING WAVEFORMS

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

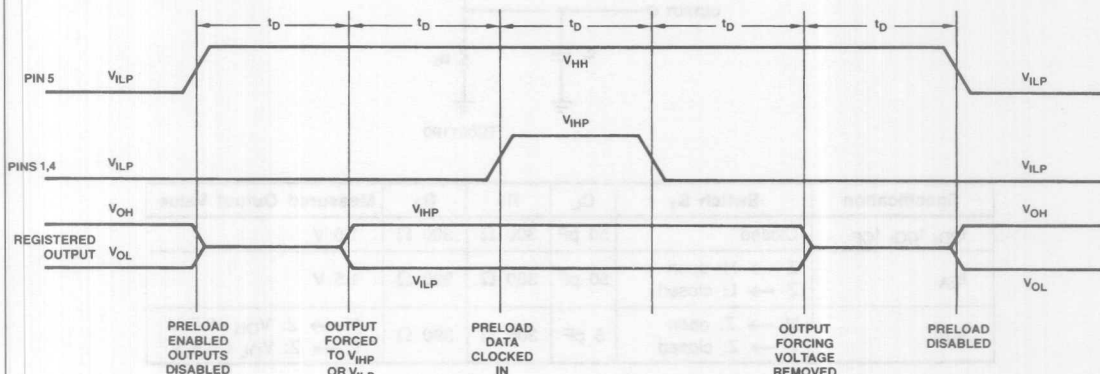
KS000010

OUTPUT REGISTER PRELOAD

The PALCE26V12H registered outputs are provided with circuitry to allow loading each register synchronously with either a HIGH or LOW. This feature will simplify testing since

any state can be loaded into the registers to control test sequencing.

The pin levels and timing necessary to perform the PRELOAD function are detailed below.



WF022295

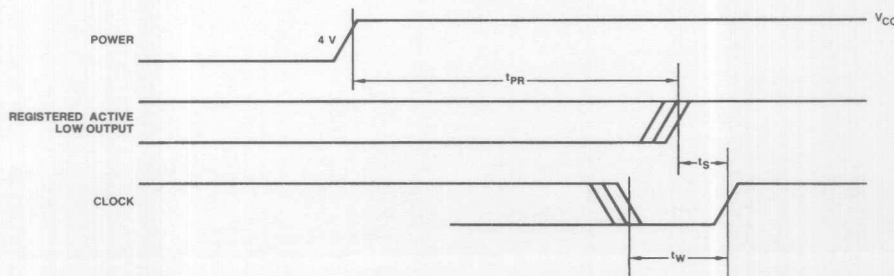
Par.	Min.	Max.	Unit	Level forced on registered output pin during PRELOAD cycle	Register Q output state after cycle
V _{HH}	10.25	10.75	V	V _{IHP}	HIGH
V _{ILP}	0	0.5	V		
V _{IHP}	2.4	5.5	V	V _{IHP}	HIGH
t _p	10		μs	V _{ILP}	LOW

POWER-UP RESET

The registered devices in the AMD PAL Family have been designed with the capability to reset during system power-up. Following power-up, all registers will be reset to LOW. The output state will depend on the polarity of the output buffer. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the asynchronous operation of the power-up reset, and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Min.	Typ.	Max.	Unit
t _{PR}	Power-Up Reset Time		600	1000	ns
t _S	Input or Feedback Setup Time	See Switching Characteristics table			
t _W	Clock Width				



WF022301

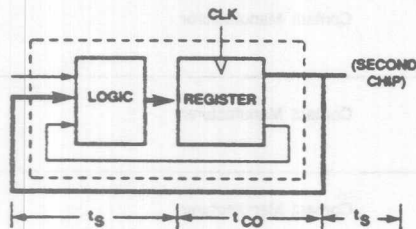
f_{MAX} PARAMETERS

The parameter f_{MAX} is the maximum clock rate at which the device is guaranteed to operate. Because flexibility inherent in programmable logic devices offers a choice of clocked flip-flop designs, f_{MAX} is specified for two types of synchronous designs.

The first type of design is a state machine with feedback signals sent off-chip. This external feedback could go back to the device inputs, or to a second device in a multi-chip state machine. The slowest path defining the period is the sum of the clock-to-output time and the input setup time for the

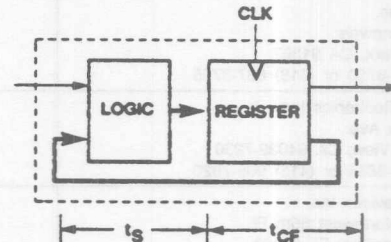
external signals ($t_S + t_{CO}$). The reciprocal, f_{MAX} , is the maximum frequency with external feedback or in conjunction with an equivalent speed device. This f_{MAX} is designated "f_{MAX} external."

The second type of design is a single-chip state machine with internal feedback only. In this case, flip-flop inputs are defined by the device inputs and flip-flop outputs. Under these conditions, the period is limited by the internal delay from the flip-flop outputs through the internal feedback and logic to the flip-flop inputs ($t_S + t_{CF}$). This f_{MAX} is designated "f_{MAX} internal."



BD008390

f_{MAX} External Feedback; $1/(t_S + t_{CO})$



BD008400

f_{MAX} Internal Feedback; $1/(t_S + t_{CF})$

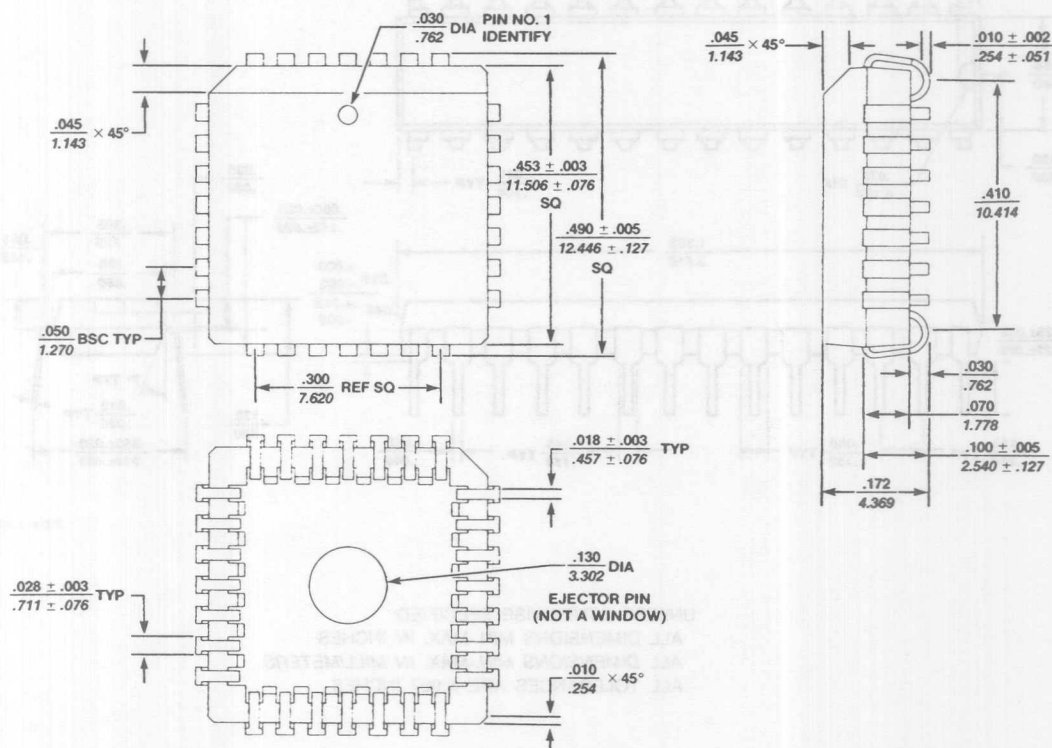
Programmers/Development Systems (Subject to change)	
MANUFACTURER	PROGRAMMER CONFIGURATION
Adams MacDonald 800 Airport Road Monterey, CA 93940 (408) 373-3607	Contact Manufacturer
Data I/O Corporation 10525 Willows Road NE PO Box 97046 Redmond, WA 98073-9746 (800) 247-5700	UniSite™ 40 rev. 2.5 Family/Pinout Code: 60-4E
Digelec Inc. 22736 Vanowen Canoga Park, CA 91307 (800) 367-8750 or (818) 887-3755	Contact Manufacturer
Kontron Electronics Inc. 630 Clyde Ave. Mountain View, CA 94039-7230 (800) 227-8834 or (415) 965-7020	Contact Manufacturer
Logical Devices Inc. 1201 E. Northwest 65th Pl. Fort Lauderdale, FL 33309 (800) 331-7766 or (305) 974-0967	Contact Manufacturer
Micropross Parc d'Activite des Pres 5, rue Denis-Papin 59650 Villeneuve-d'Ascq (20) 47.90.40	Contact Manufacturer
Stag Microsystems Inc. 1600 Wyatt Dr. Suite 3 Santa Clara, CA 95054 (408) 988-1118	Contact Manufacturer
Varix Corporation 1210 E. Campbell Rd. Suite 100 Richardson, TX 75081 (214) 437-0777	Contact Manufacturer
MANUFACTURER	SOFTWARE DEVELOPMENT SYSTEM
Advanced Micro Devices, Inc. 901 Thompson Place Sunnyvale, CA 94088-3453 (800) 222-9323	PALASM® 2 Software, rev. 2.23D and later
Data I/O Corporation 10525 Willows Road NE PO Box 97046 Redmond, WA 98073-9746 (800) 247-5700	ABEL™ Software, rev. 3.1 and later
Logical Devices Inc. 1201 E. Northwest 65th Pl. Fort Lauderdale, FL 33309 (800) 331-7766 or (305) 974-0967	CUPL™ Software, (contact manufacture)
UniSite™ and ABEL™ are trademarks of Data I/O Corporation CUPL™ is a trademark of Logical Devices Inc.	

28P Molded SKINNYDIP®



PHYSICAL DIMENSIONS (Cont'd.)

28J Molded Chip Carrier



PID# 11757-007A

UNLESS OTHERWISE SPECIFIED:
 ALL DIMENSIONS MIN.-MAX. IN INCHES
 ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
 ALL TOLERANCES ARE $\pm .007$ INCHES

PALASM 2 SOFTWARE SUPPORT FOR THE PALCE26V12

About this Section

This section describes PALASM 2 software special considerations for the PALCE26V12 device. It is intended as a supplement to the PALASM 2 software user documentation in part 4 of the 1988 PAL Device Data Book. If you do not already have the Data Book, contact your local AMD sales office for a copy.

PALASM 2.23D and later versions support the PALCE26V12 device.

In this section, *fuse* refers to one of the programmable bits.

Boolean Equation Design Entry

1. The PALCE26V12 has 28 physical pins, 1 global SET/RESET node and 12 buried nodes. This pin list reflects the pinout shown in the logic diagram in this data sheet.

Example

```
CHIP                26V12_Example        PALCE26V12

;PINS

;1   2   3   4   5   6   7   8   9  10  11  12  13  14
CLK1 I1 I2 CLK2 I4 I5 VCC I6 I7 I8 I9 I10 I11 I12

;15  16  17  18  19  20  21  22  23  24  25  26  27  28
O0  O1 O2  O3  O4  O5 GND O6 O7 O8 O9 O10 O11 I13

;NODES

; 1
INIT

;2   3   4   5   6   7   8   9  10  11  12  13
R0  R1 R2  R3  R4 R5 R6 R7 R8 R9 R10 R11
```

Note: Lines beginning with a semicolon are comments and are ignored by the software.

Note: Refer to *Functional Equations*, Section 4.1.3.4 in Chapter 4 of the PAL Data Book for detail on the programmable set and reset functions.

2. If your design does not require the definition of the 13 buried nodes on the device, you can define pin names for the pins only, leaving out *all* 13 nodes. PALASM 2 software automatically assigns the name NC (no connect) to all the nodes. You cannot, however, include some nodes in your pin list and leave out the unused ones. If you use some nodes, you must define the others as NC.

Note that without the buried nodes, the PALCE26V12 must be designed like a PAL22V10 device.

See items 5, 6 and 7 in this section for more information on defining buried nodes in equations.

3. Each macrocell on the device allows eight output configurations:
 - Combinatorial output, I/O combinatorial feedback/active-low and active-high output
 - Combinatorial output, registered feedback/active-low and active-high output
 - Registered output, registered feedback/active-low and active-high output
 - Registered output, I/O registered feedback/active-low and active-high output

The logic diagram in this data sheet illustrates the PALCE26V12 macrocell fuse settings. Table 1 defines each fuse.

Table 1

Fuse Functionality for the PALCE26V12 Macrocell

Fuse	Type	Setting	Configuration
S0	Polarity	0	Active-Low
		1	Active-High (default)
S1	Register	0	Registered Output
	Bypass	1	Combinatorial Output (default)
S2	Clock Select	1	Clock1 from Pin1 (default)
		0	Clock2 from Pin4
S3, S1	Feedback Control	0,1	Registered Feedback from /Q
		1,0	Registered Feedback from /Q
		1,1	I/O Feedback from Pin
		0,0	I/O Feedback from Pin

Note: S3 defaults to 1.

Figures 4 and 5 illustrate the Boolean equations for PALASM 2 syntax along with the output configurations and fuse settings. For items 4 through 7 below, please refer to Figures 4 and 5.

- The equations in Figures 4 and 5 assume that the pins in the pin list are all active-high as shown in item 1 in this section. The polarity of the output depends on the polarity of the pins in the pin list and Boolean equations. Refer to *Polarity*, Section 4.2 in Chapter 4 of the PAL Data Book for a detailed discussion on output polarity.

Notice that based on the active-high R nodes in the pin list, the R node feedback must be active-low in all the equations.

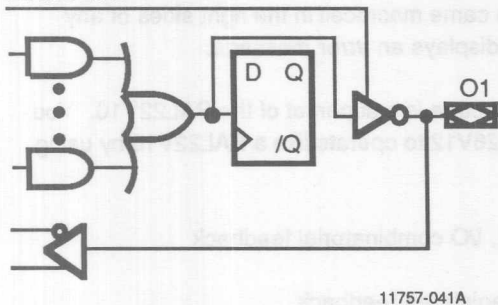
- In Figures 4 and 5, notice that pairs of identical equations are defined at O1 and R1 in the output configurations 2 and 4. Currently, the software *requires* that identical equations be defined at the O pin and R node for these configurations. Future versions of PALASM software will simplify this.

6. Feedback, both combinatorial and registered, is selected by using the O pin or R node in the right side of the equation. The equations in Figures 4 and 5 show the feedback in bold type. If you use both the O and R feedback from the same macrocell in the right sides of any equations, the software displays an error message.
7. The PALCE26V12 architecture is a superset of the PAL22V10. You can program the PALCE26V12 to operate like a PAL22V10 by using configurations 1 and 3:
 - Combinatorial output, I/O combinatorial feedback
 - Registered output, registered feedback

In addition, your design defaults to a PAL22V10 design if you do not enter a node equation at R. When you define output pin equations alone, the software automatically selects I/O feedback for combinatorial output equations and registered feedback for registered output equations (i.e., S3 defaults to 1). You can configure all or some of the macrocells to operate like a PAL22V10 design.

**Configuration 1: Combinatorial Output, I/O Combinatorial Feedback
(PAL22V10 Compatible)**

Active Low



11757-041A

Equations

$$/O1 = I1 * I2 * I4$$

$$/O2 = I1 * /O1 * I4$$

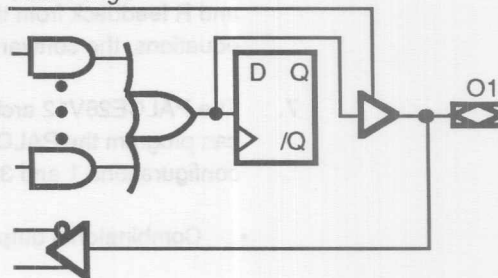
Fuse Settings

$$S0 = 0$$

$$S1 = 1$$

$$S3 = 1$$

Active High



11757-042A

Equations

$$O1 = I1 * I2 * I4$$

$$O2 = I1 * O1 * I4$$

Fuse Settings

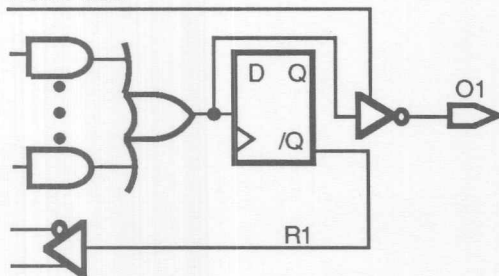
$$S0 = 1$$

$$S1 = 1$$

$$S3 = 1$$

Configuration 2: Combinatorial Output, Registered Feedback

Active Low



11757-043A

Equations

$$/O1 = I1 * I2 * I4$$

$$/R1 = I1 * I2 * I4$$

$$/O2 = I1 * /R1 * I3$$

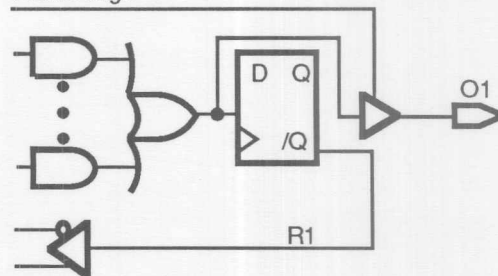
Fuse Settings

$$S0 = 0$$

$$S1 = 1$$

$$S3 = 0$$

Active High



11757-044A

Equations

$$O1 = I1 * I2 * I4$$

$$/R1 = I1 * I2 * I4$$

$$O2 = I1 * /R1 * I4$$

Fuse Settings

$$S0 = 1$$

$$S1 = 1$$

$$S3 = 0$$

Figure 4

Combinatorial Output Configurations

8. The two clock pins on the device allow you to select either or both of the clock inputs for registered configurations. The software indicates an error if a clock function is defined for a combinatorial output. If no clock function is defined for a registered output, the software defaults to clock1 from pin1.

The syntax for the clock functional equation follows.

Syntax

Output_Pin.CLKF = CLK1 (default)

Output_Pin.CLKF = CLK2

Note: CLK1 and CLK2 can also be used as input pins for combinatorial designs.

State Machine Design Entry

For the current version of the software, the use of manual state assignment is recommended over automatic state assignment.

If you choose the automatic state assignment option, do not name the output pins NC (no connect). To avoid errors, use the name NC only for buried nodes. You can use dummy names for unused output pins.

Refer to *State Assignments*, Section 5.2.3.2, in Chapter 4 of the PAL Data Book for a description of manual and automatic state assignment.